IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) ~~An improved~~ A digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals; and

a feedback ~~means~~ circuit interconnecting said plurality of memory devices and cross-coupling signals produced by said plurality of memory devices.

2. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 1, further comprising:

a common frequency reference source in communication with said plurality of memory devices, said common frequency reference source ~~for~~ driving said plurality of memory devices.

3. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim ~~2~~ 1, wherein said multiple timing signals include at least one signal selected from the group consisting of an RF carrier signal, a data bit-rate signal, a data chip-rate signal, a data frame-rate signal, ~~and~~ a data burst-rate signal ~~or~~ and a packet-rate signal.

4. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2, wherein said multiple timing signals are integrally or fractionally related in frequency, phase or both frequency and phase.

5. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2, wherein said multiple timing signals are rationally ~~multiply~~ related in frequency and/or phase.

6. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim ~~2~~ 3, wherein said multiple timing signals satisfy a ~~the~~ relationship

$$f_1 = M \cdot f_2 = M \cdot N \cdot f_3$$

wherein f_1 is said RF carrier signal; f_2 is said data bit-rate signal; f_3 is said data frame-rate signal; and M and N are positive rational numbers.

7. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2, wherein said common frequency reference source includes ~~is~~ an oscillator controlled by a crystal, SAW device, ceramic resonator, mechanical resonator, dielectric resonator, or external source.

8. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2, wherein said common frequency reference source uses edge-triggered synchronous logic.

9. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim ~~2~~ 1, wherein ~~said~~ signals cross-coupled by said feedback ~~means~~ circuit

include at least one ~~signal~~ member selected from the group consisting of error signals~~, output signals, and both error~~ and output signals.

10. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 1, wherein ~~said~~ signals cross-coupled by said feedback ~~means are~~ circuit include analog signals.

11. (Currently Amended) The ~~improved~~ digital-data receiver synchronization of claim 1, wherein ~~said~~ signals cross-coupled by said feedback ~~means are~~ circuit include digital signals.

12. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 1, wherein said plurality of memory devices ~~are~~ include phase-locked loops.

13-26. (Canceled)

27. (Currently Amended) ~~The~~ A method of providing improved digital-data receiver synchronization comprising ~~the steps of~~:

providing a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector, each of said plurality of memory devices providing an output comparison signal; and~~,~~

interconnecting said plurality of memory devices with a feedback ~~means~~ circuit ~~for~~ that cross-couples ~~cross-coupling~~ said output comparison signal~~s~~ produced by each of said plurality of memory devices.

28. (Currently Amended) The method according to claim 27, further comprising ~~the step of~~:

connecting a common frequency reference source to ~~with~~ said plurality of memory devices, said common frequency reference source ~~for~~ driving said plurality of memory devices.

29. (Canceled)